Advanced CMOS Spectrometer SoCs for Next Generation Spaceborne Radio-Telescopes

(but probably useful for Earth Science too)

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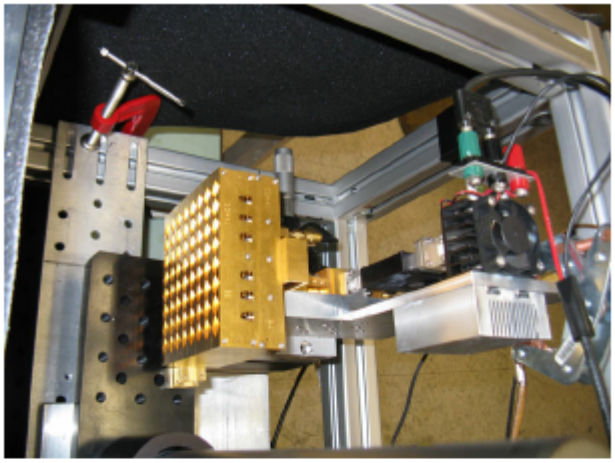
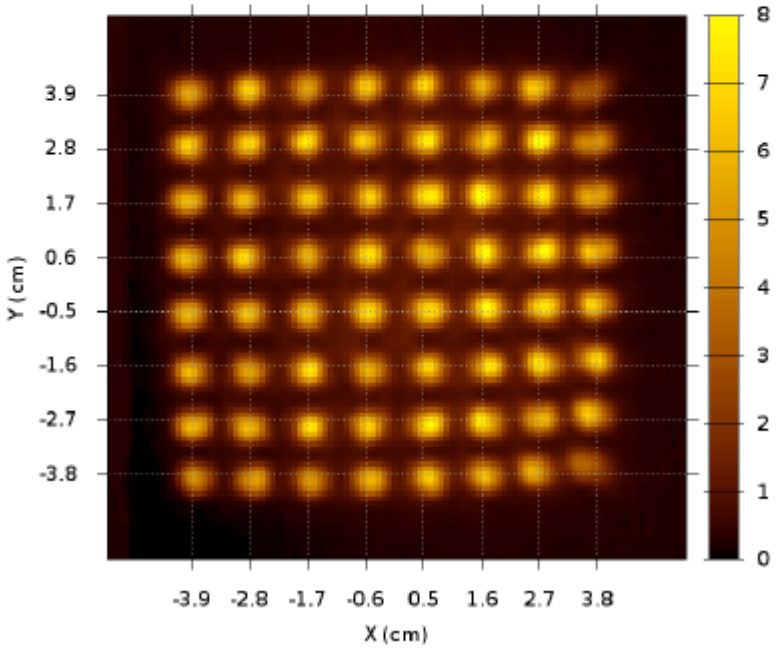
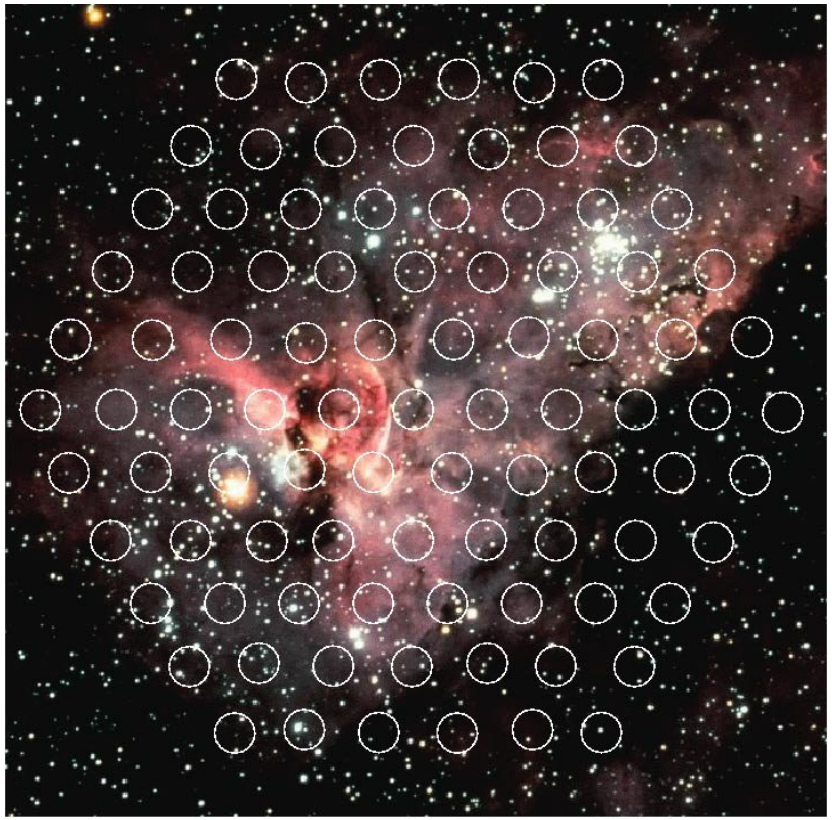
Motivations

- Enable spectrometer systems far-beyond what is possible with existing FPGA based technology.
- Develop a complex CMOS SoC for spectrometer back-end processing that has everything needed on-chip to operate in laboratory, airborne and spaceflight environments.
- Emphasis on high integration capability and low power consumption to enable back-end processing for large heterodyne arrays.
- Employ advanced SoC practices and architectures of dynamic and background calibration, debugging, internal clock and power management, to rapidly adapt to radiation and extreme temperature environments.

Our Major Customer (sorry Earth Science)

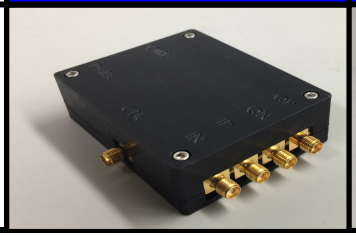
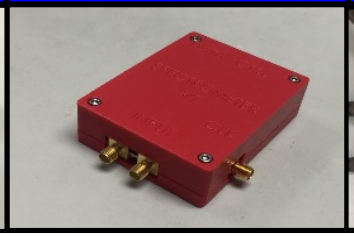
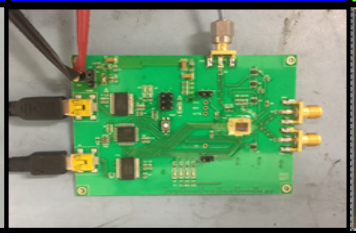
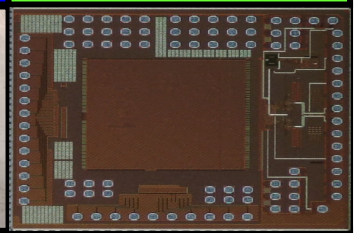




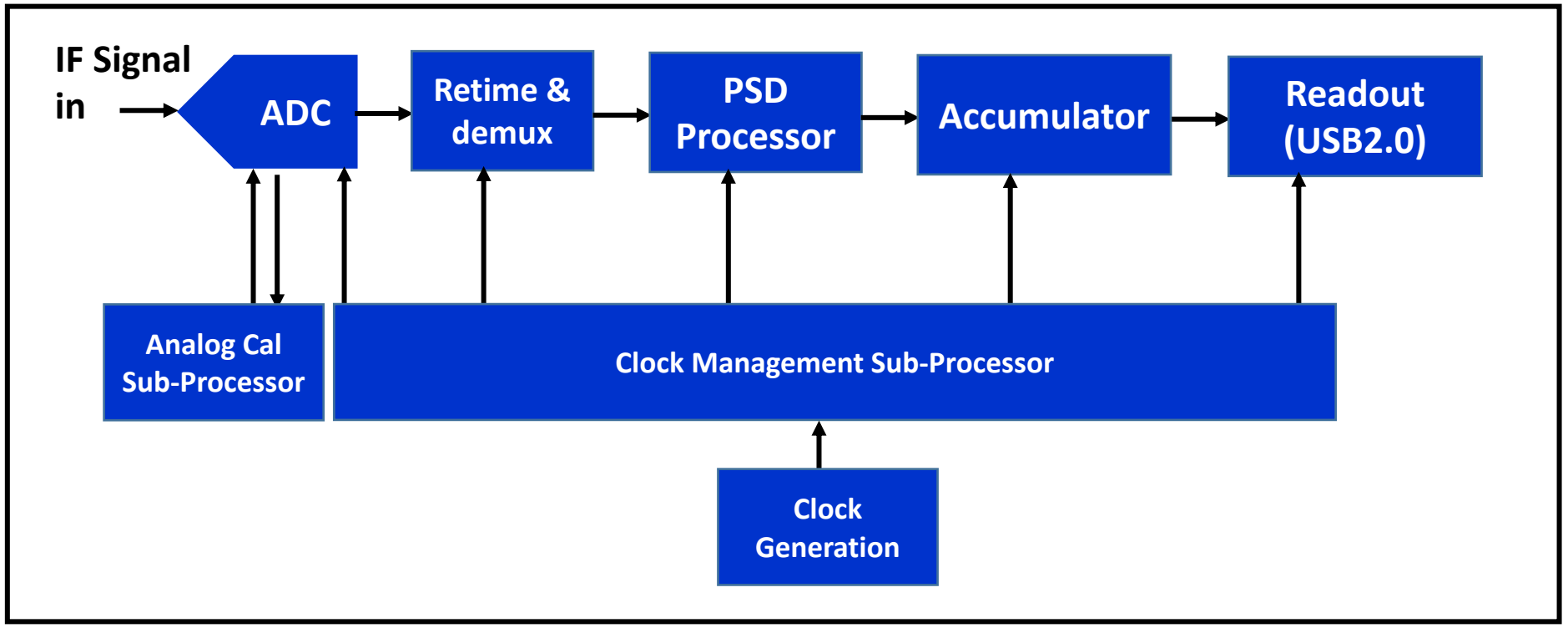


- **Astronomers want big-pixel counts in spaceborne telescopes. This means extremely low power back-end spectrometer processing!**

UCLA – JPL Spectrochip Product Line

Design Parameter	Demonstrated CMOS Spectrometer Systems			
	Spectrochip SII Spectrometer (UCLA/JPL) 2015 [1]	Spectrochip SVI Spectrometer (UCLA/JPL) 2016 [2]	Spectrochip SVII Spectrometer (UCLA/JPL) 2017 [3]	Spectrochip SVIII Spectrometer (UCLA/JPL) Available Late 2019
Processor Bandwidth (MHz)	1000	1500	3000	6000
Channel Count (#)	512	1024	4096	8192
FFT Window Type	Rectangle	Poly-Phase	Hanning	PFB
FFT Format	IQ	Real	Real	Real
Bit Resolution (#)	4	3	3	3
Power (W)	0.56 W	0.86 W	1.75 W	1.9 W
Size (cm^3)	10x8x2 cm	10x8x2 cm	10x8x2 cm	6x8x2 cm
Packaging Technique	Wire-Bond	Ribbon-Bond	Ribbon-Bond	Flip Chip
Weight (Kg)	0.12 Kg	0.12 Kg	0.12 Kg	0.12 Kg
Core Technology	65nm CMOS	65nm CMOS	65nm CMOS	28nm HPC CMOS
				

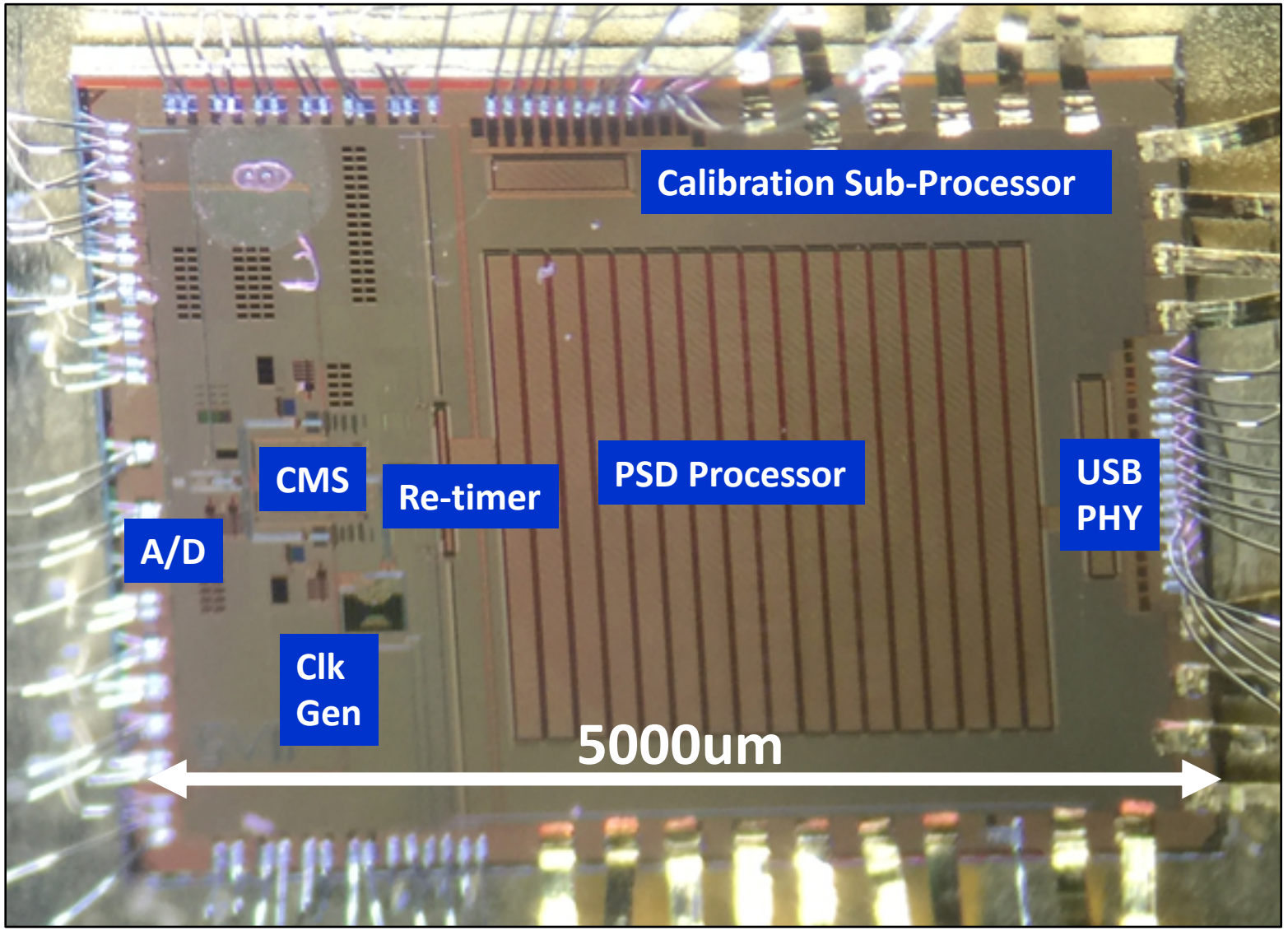
High Level CMOS SoC Architecture



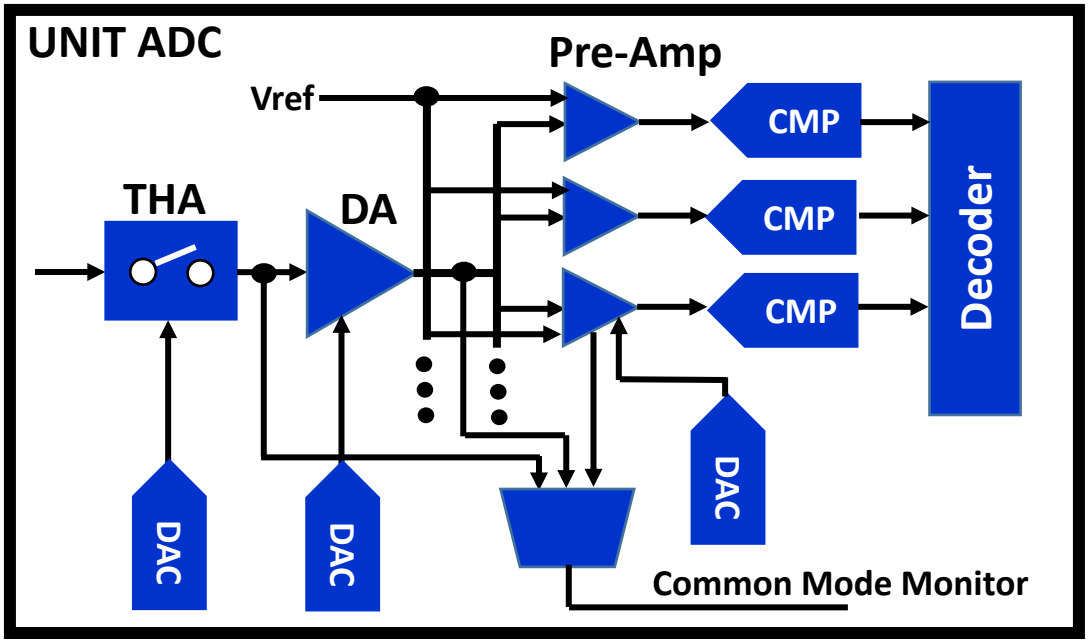
- Beyond the conventional processing chain of ADC/PSD/Readout we also have dedicated calibration sub-processors for clock management and analog calibration within our SoC allowing robust operation at 6GS/s over a wide range of temperature, radiation and fabrication process conditions.

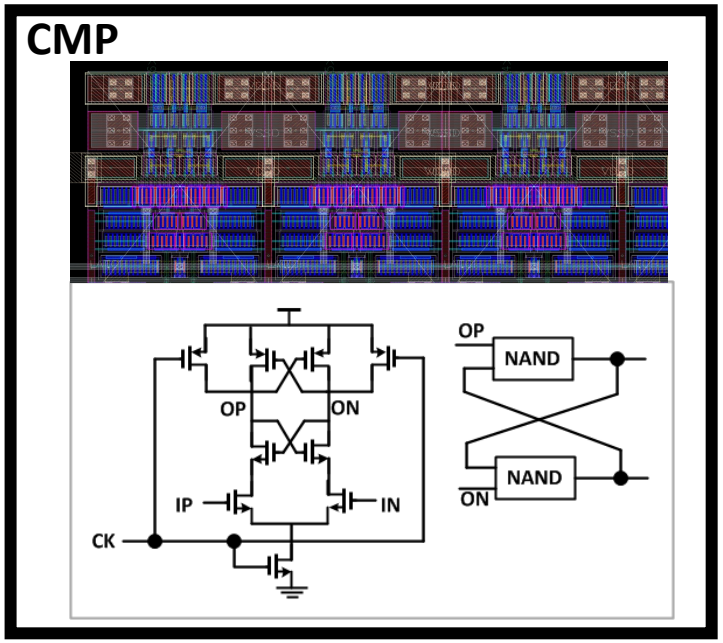
- "Build now, calibrate later" philosophy. Just like Broadcom.

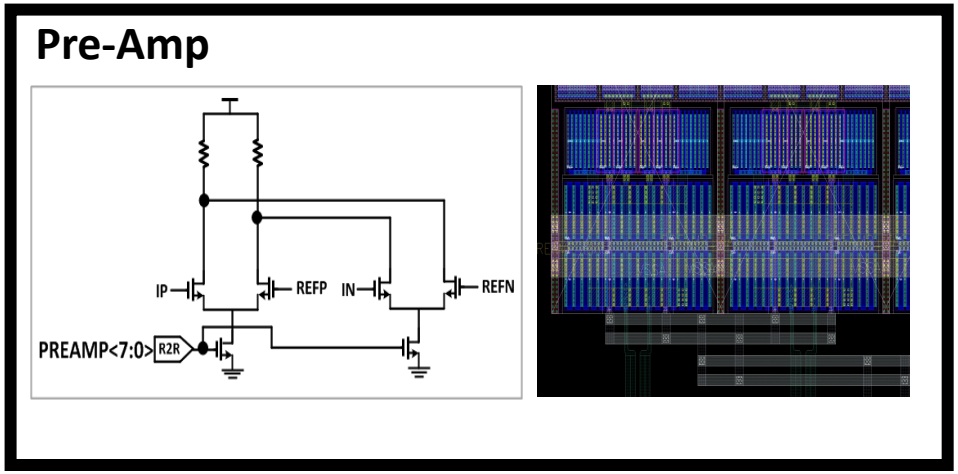
CMOS SVII Spectrometer Processor



Front-End Unit ADC Block Diagram

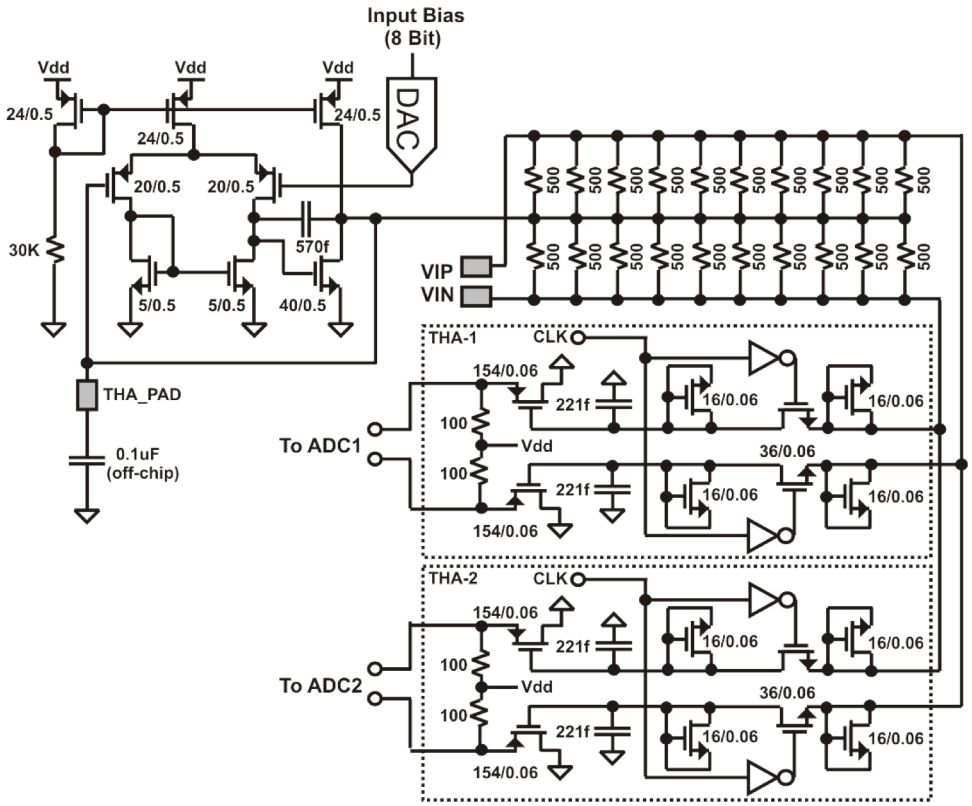


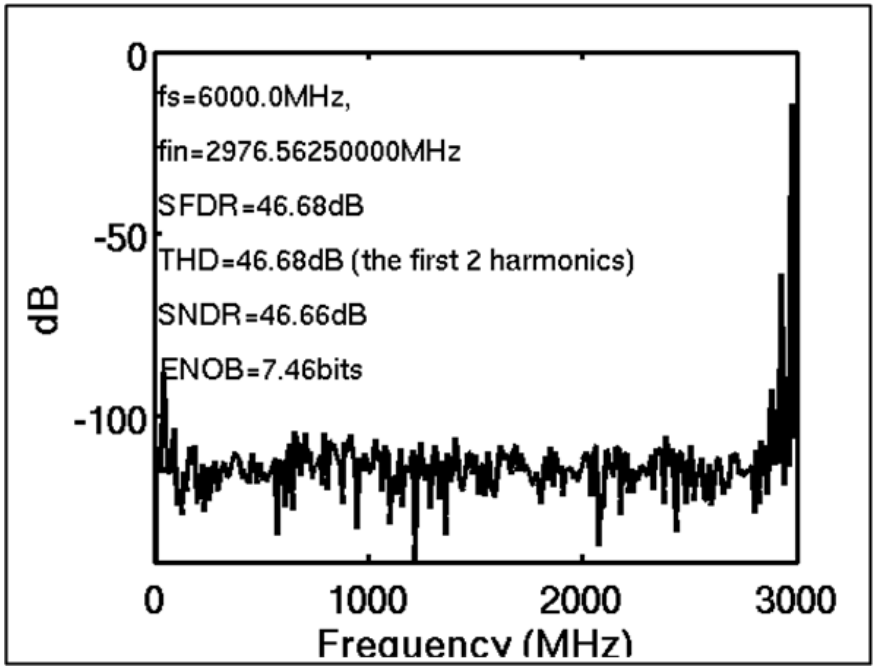




- Fairly typical structures similar to an 802.11 product.
- Addition of Common mode monitoring and digital trimming of all DC bias using 8-bit DACs throughout the analog stages.

ADC Input THA Network Details

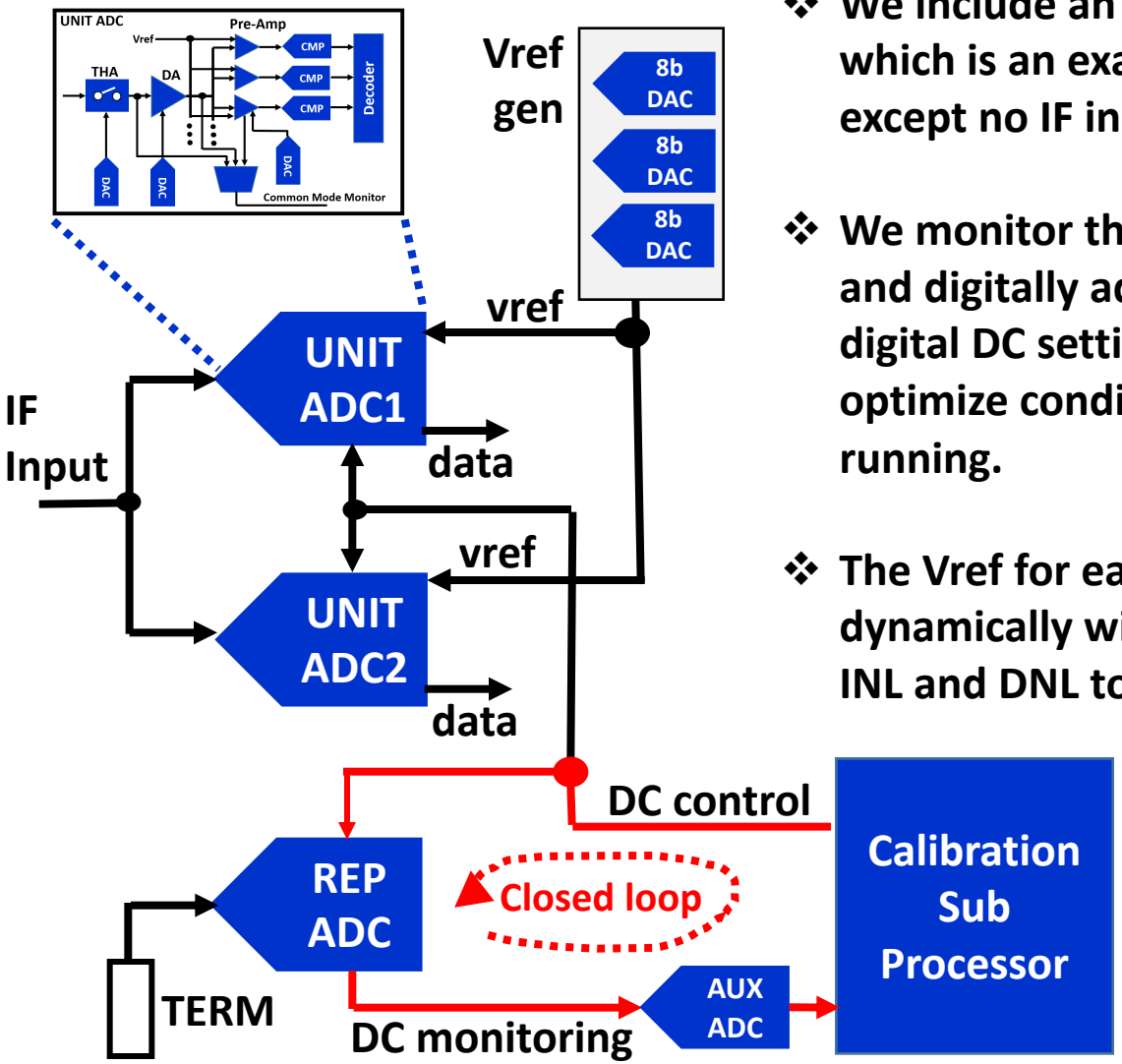




- **Input network is a typical high-speed track-and-hold structure with digital common mode calibration that is driven by software running on the calibration sub-processor.**

- **Achieving about a 7.4 bit ENOB after calibration across corners and temperature.**

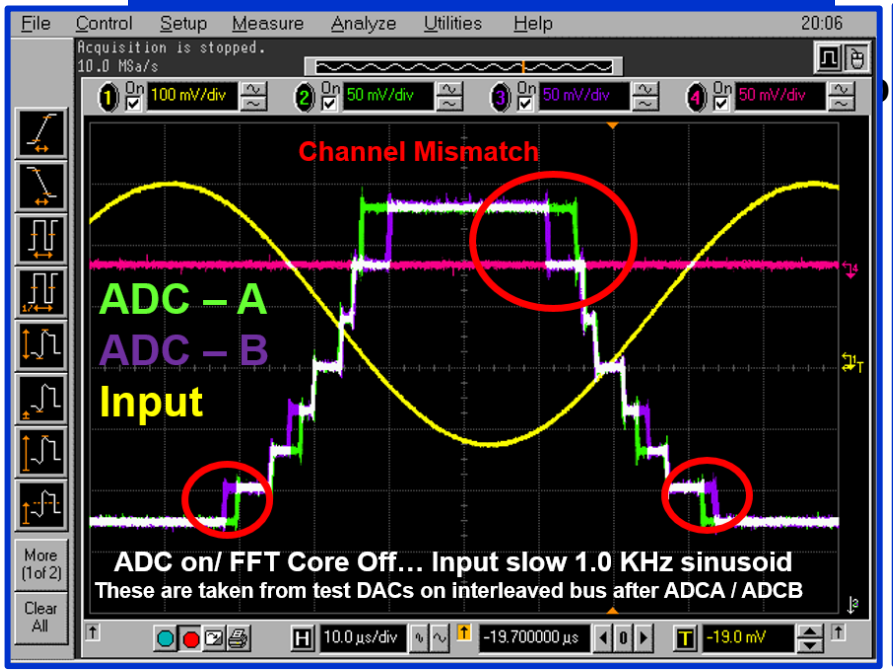
ADC Global Calibration Architecture



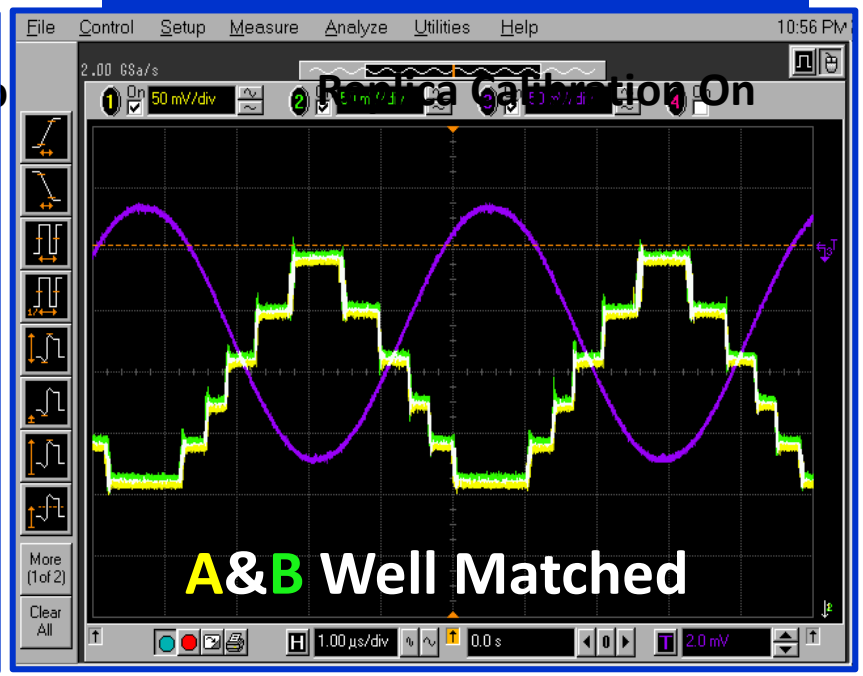
- We include an extra ADC called a “Replica” which is an exact duplicate of the real ADCs except no IF input signal is applied.
- We monitor the DC conditions of the replica and digitally adjust all 3 ADCs, with the same digital DC settings in closed loop, allowing us to optimize conditions in the ADC while it’s running.
- The Vref for each flash ADC level is generated dynamically with a set of 7 8-bit DACs. Allows INL and DNL to be calibrated on the fly also.

ADC Global Calibration Example

ADC Before Self-Calibration

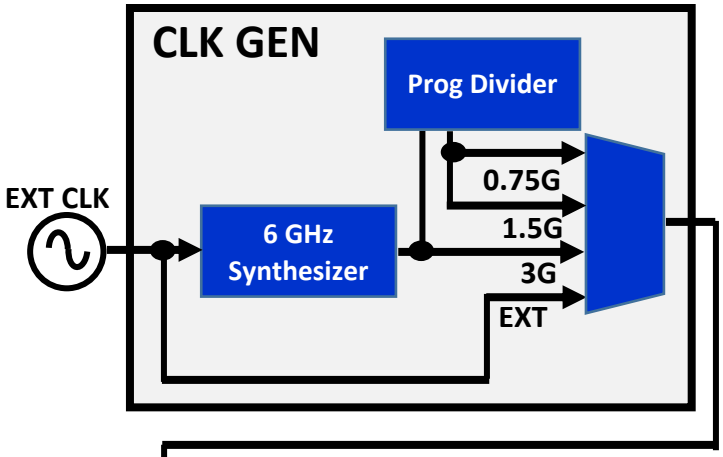


ADC After Self-Calibration

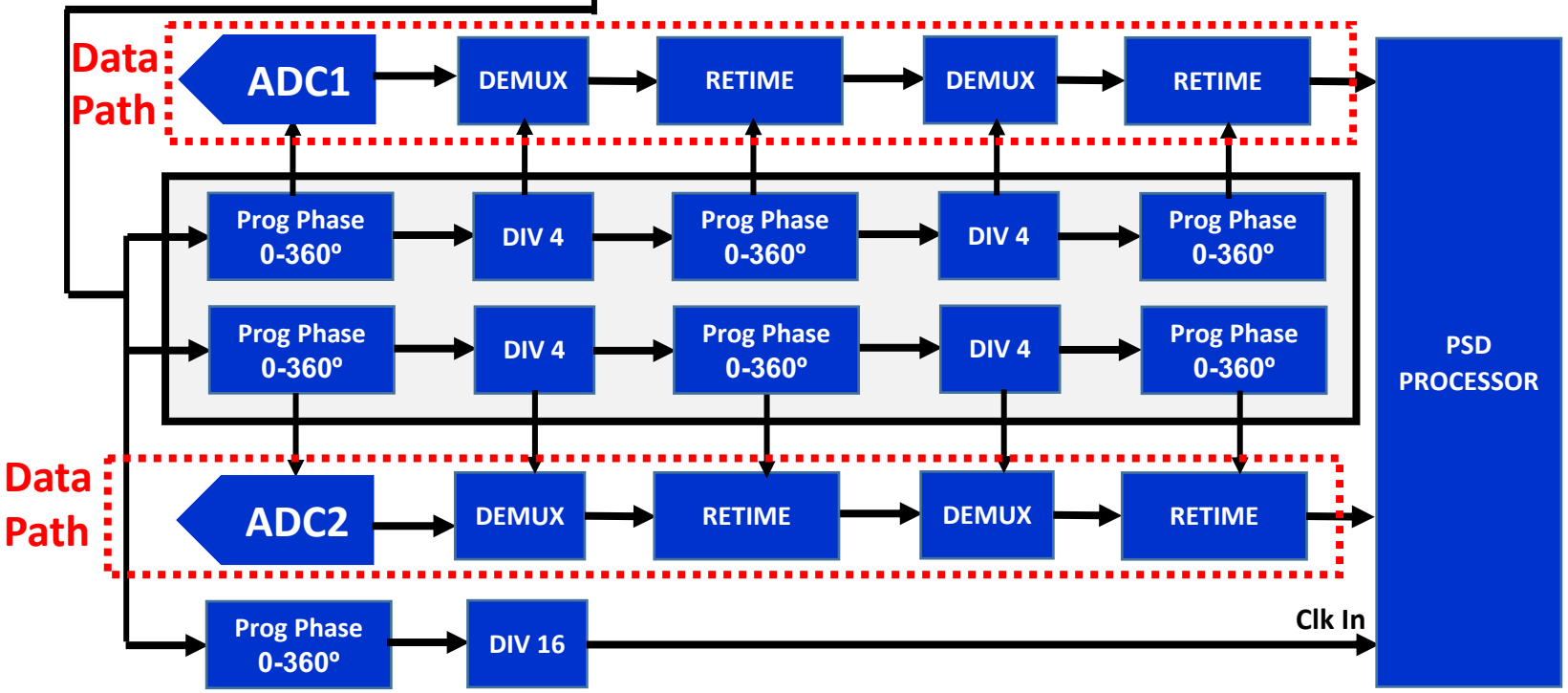


- Mismatch of ADC sub-channels is the major issue in interleaved ADCs.
- By monitoring the induvial interleaved ADC outputs before and after the calibration is applied we can see that calibration sub-processor is working correctly.

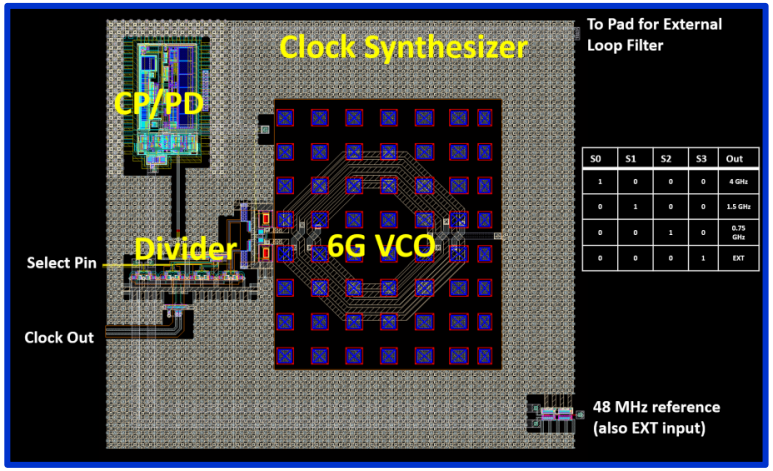
SVII Clocking Architecture

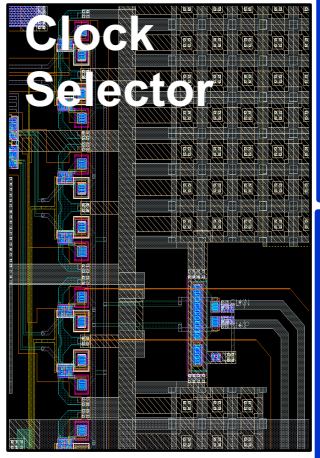


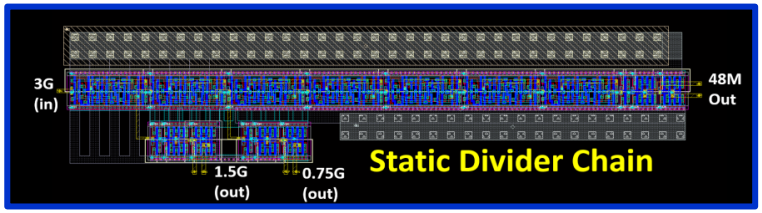
- At high speed, timing needs to be robust. We use an army of clock-tuners that adjust the clock phase throughout the chip to align phases of each individual stage in the data pipeline to ensure setup and hold margins are met.
- Main clock is derived from an internal synthesizer and is selectable at full, half, quarter, or arbitrary EXT speed.

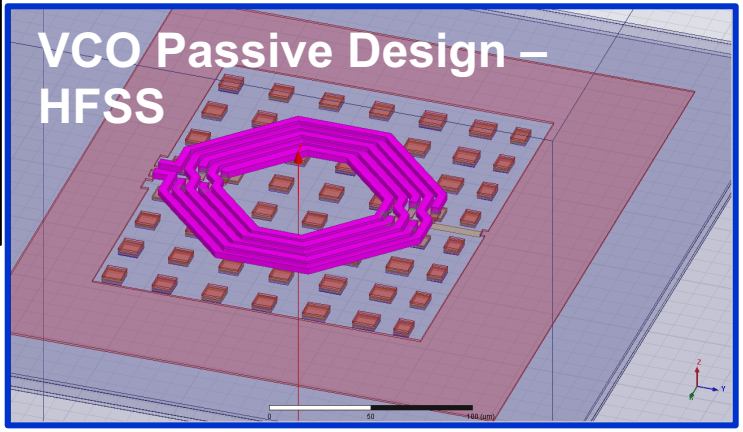


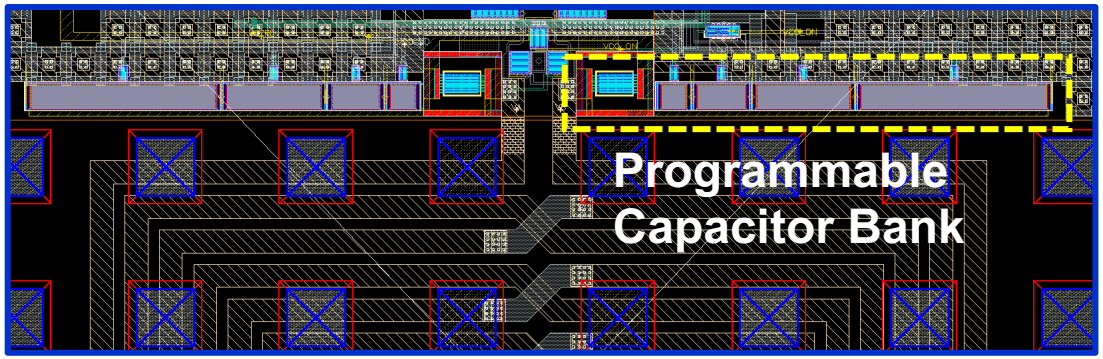
Clock Generation System





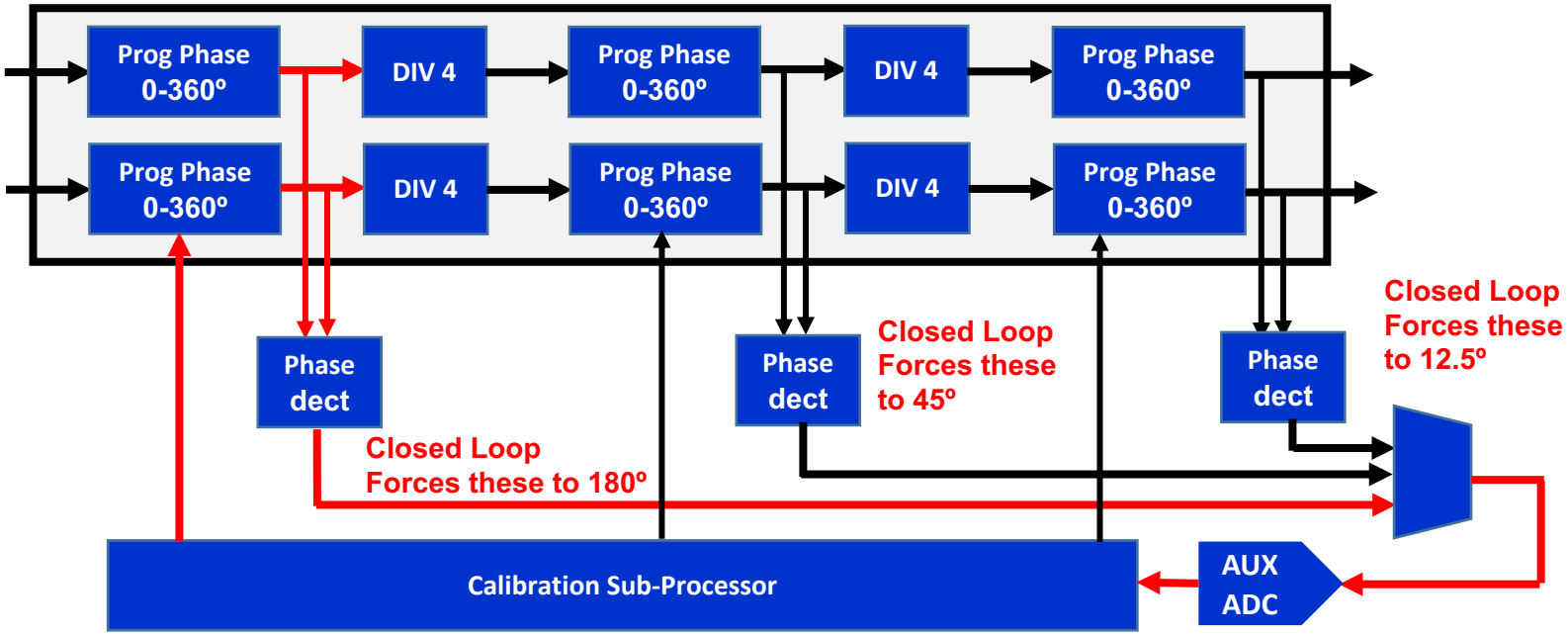






- Integrated type-II phase-lock loop based frequency synthesizer with built in microwave VCO, charge pump, phase detector and loop filter.
- Additionally, digitally selected capacitor banks allow the VCO frequency band to be trimmed to ensure we cover 6 GHz across all temperatures and process conditions
- Software on the cal-sub-processor monitors vctrl and selects the correct cap bank.

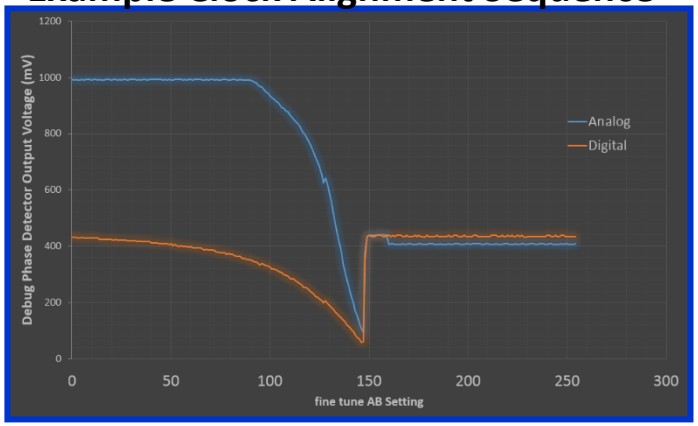
Clock Alignment Calibration



- Clock system contains phase detectors between key points which the calibration sub-processor uses to automatically set the digital phase shifters and align the clock edges in the data path and processor core.

- Software on the calibration sub-processor defines what each clock phase needs to be. Calibration runs in the background, adapting for temperature and other drifts.

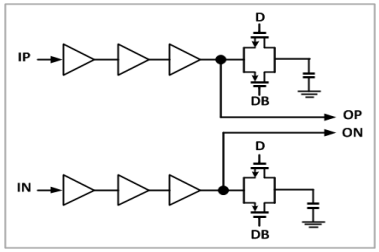
Example Clock Alignment Sequence



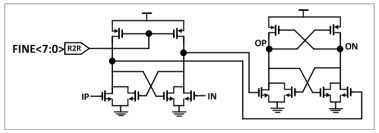
Data Alignment and Retiming Pathways

Delay Tuner

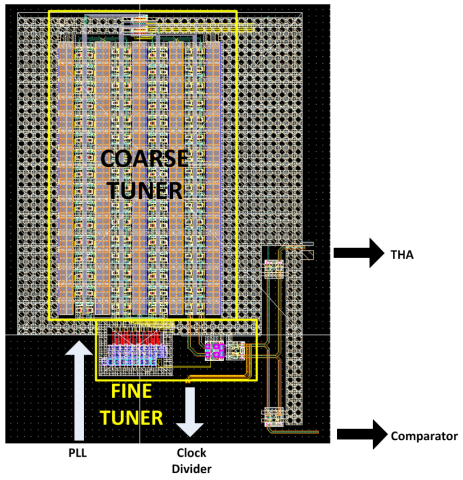
Coarse Unit Cell



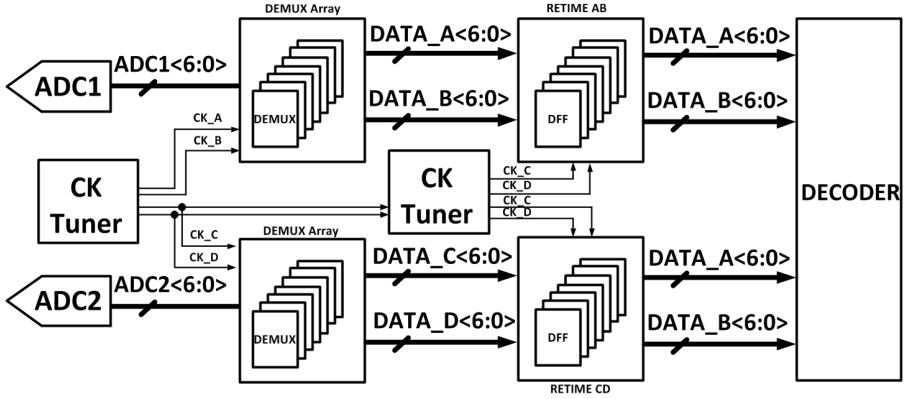
Fine Unit Cell

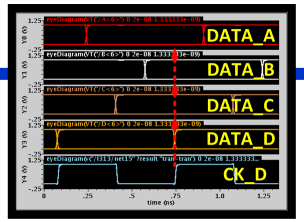


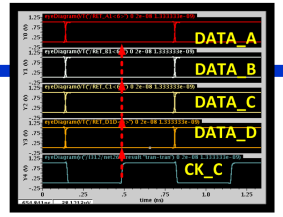
Delay tuner module

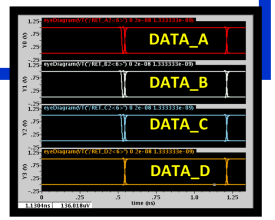


Retiming System Block Diagram

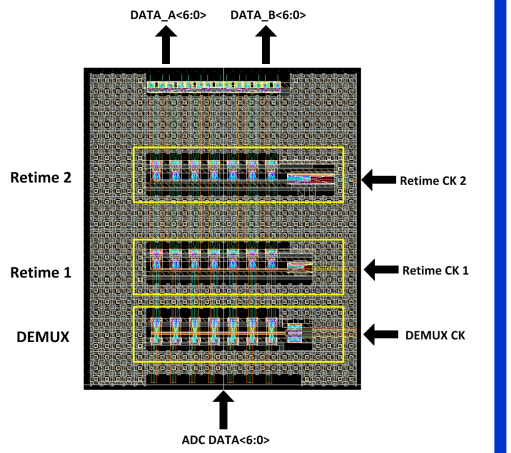




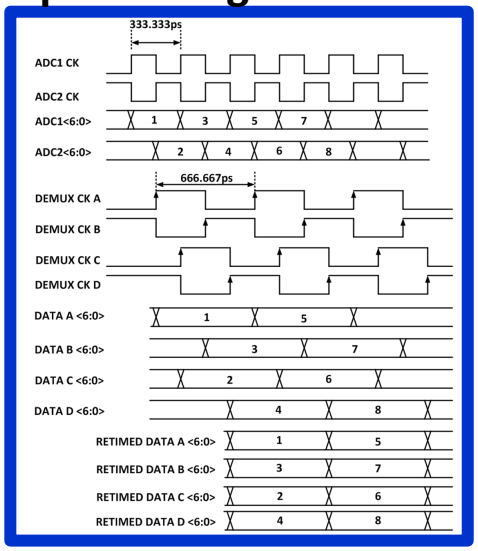




Re-timer

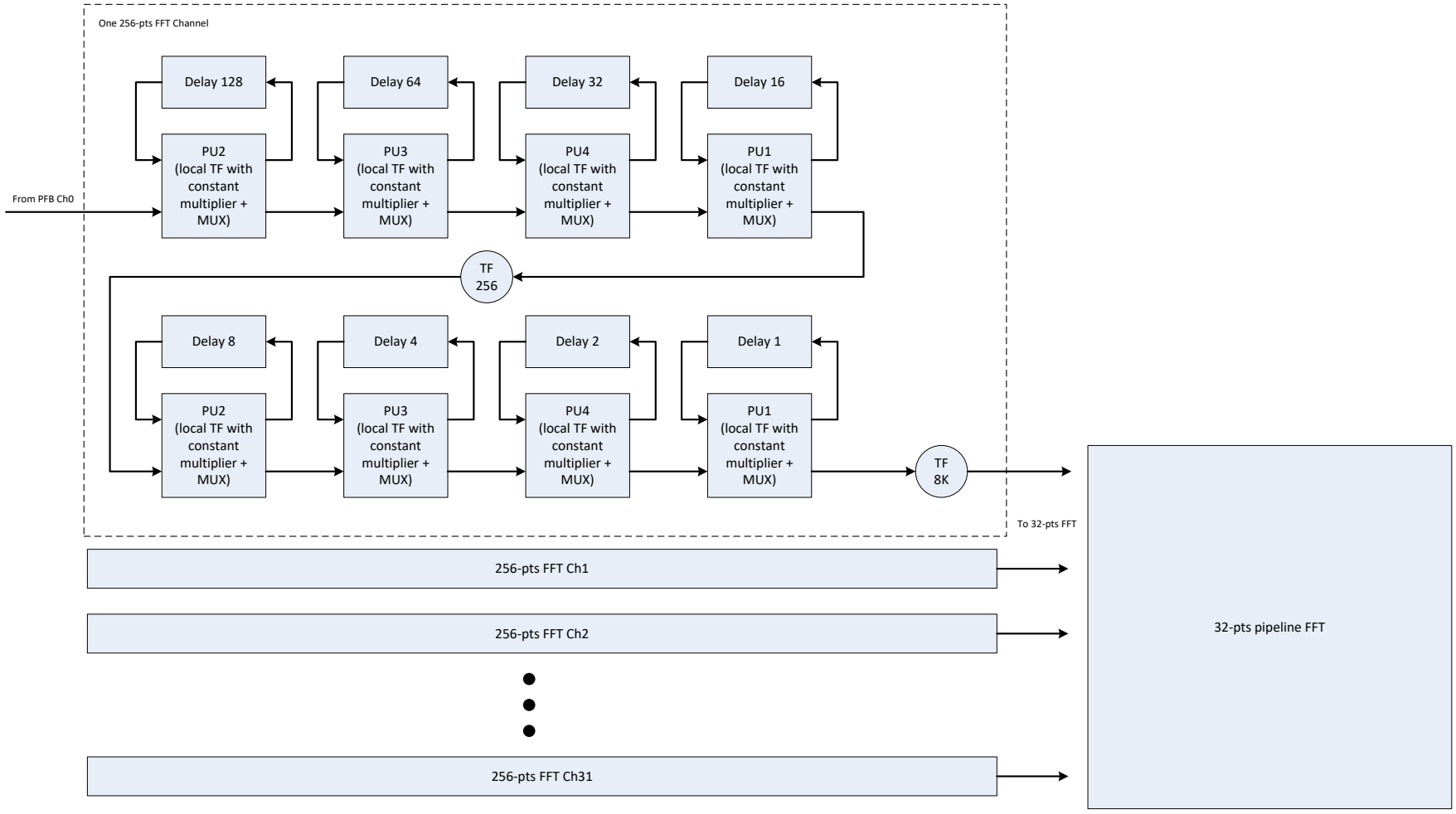


Optimal Edge Schedule



- Retiming pathway brings all the data to the same edge to be picked up by the PSD processor core.
- Calibration sub-processor is programmed with the optimal data schedule and adjusts phases throughout the pathway in closed loop to establish robust timing.

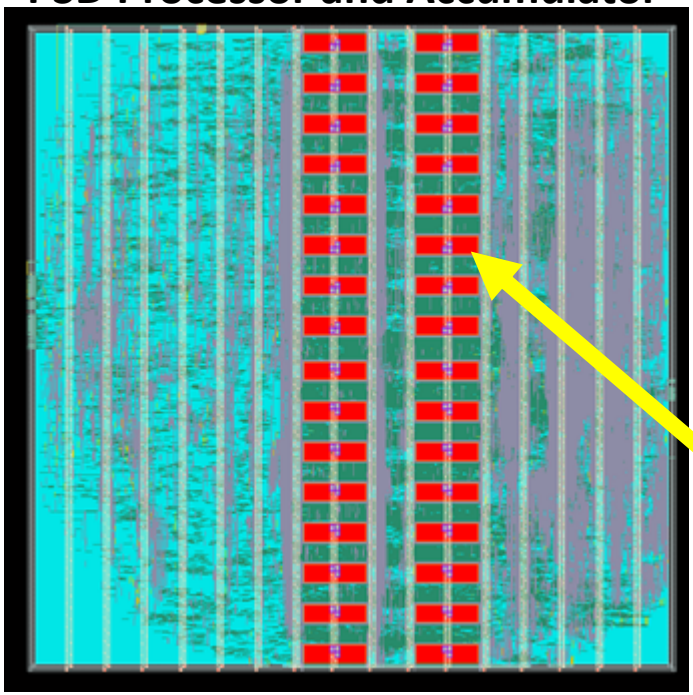
FFT Processor Architecture

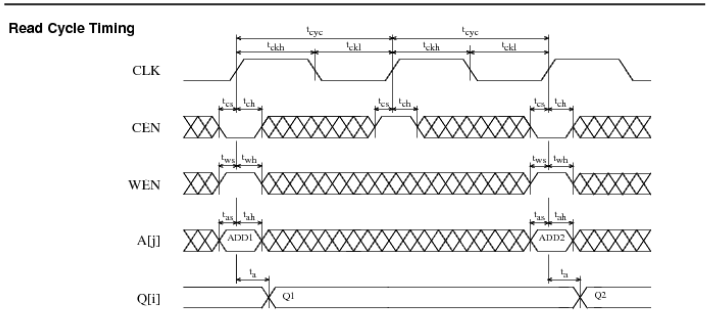


- **Block diagram is pretty much straight from the textbook. 32 parallel 256 point FFTs followed by a 32-pt pipeline FFT.**

Integration SRAM Accumulator

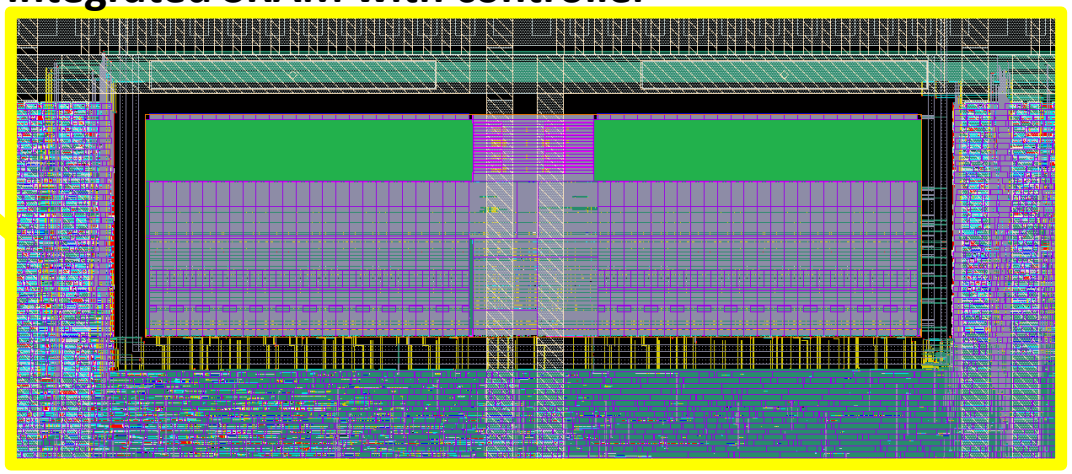
PSD Processor and Accumulator





Pin	Symbol	Fast Process 1.1V, -40°C	
		Min	Max
Cycle time[4]	t_{cyc}	0.664	
Access time[1,2,4]	t_a	0.179	
Address setup	t_{as}	0.164	
Address hold	t_{ah}	0.090	
Data setup	t_{ds}	0.074	
Data hold	t_{dh}	0.087	
Chip enable setup	t_{cs}	0.115	
Chip enable hold	t_{ch}	0.090	
Write enable setup	t_{ws}	0.082	
Write enable hold	t_{wh}	0.127	
Clock high	t_{ckh}	0.023	
Clock low	t_{ckl}	0.037	
Clock rise slew	t_{ckr}		1.000
Output load factor[3]	K_{load}		0.186
RETN to Q delay	t_{retnq}	0.188	
RETN setup	t_{retns}	0.117	
RETN hold	t_{retnh}	0.092	
CEN to RETN hold	t_{cen_retnh}	0.157	
RETN to CEN hold	t_{retn_cenh}	0.769	

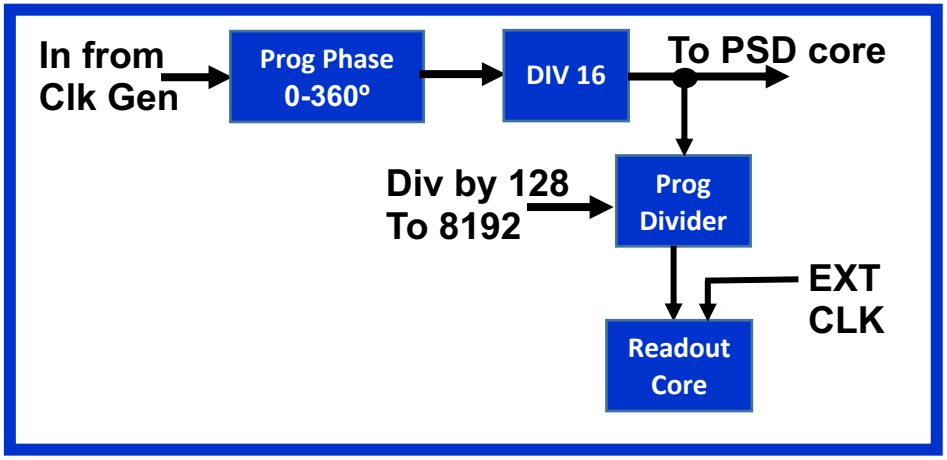
Integrated SRAM with controller



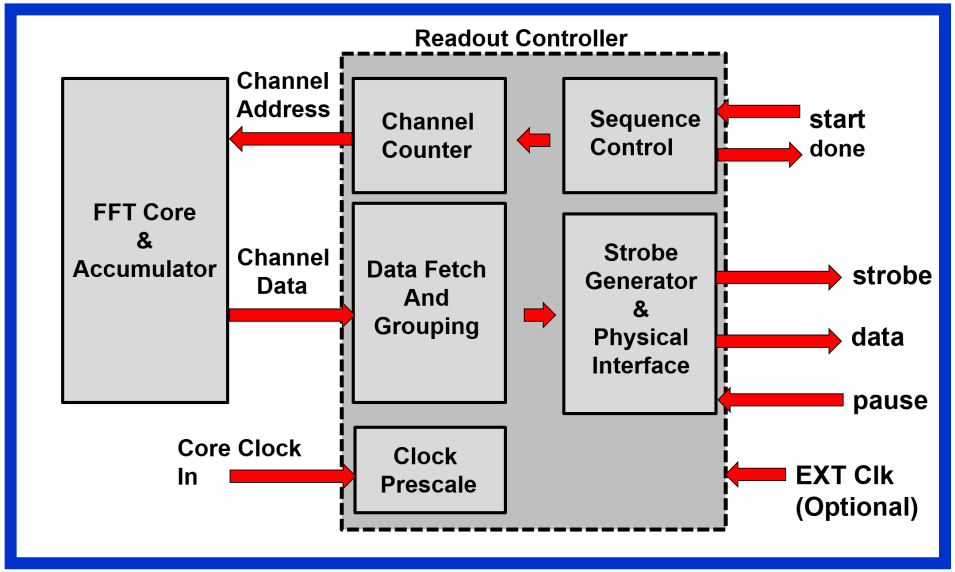
- We use integrated SRAMs to store and accumulate the results of the PSD processor. Control logic controlled by the main chip firmware sets the number of accumulations so that the integration time is fully programmable.

Readout Interface Architecture

Clock Scheme

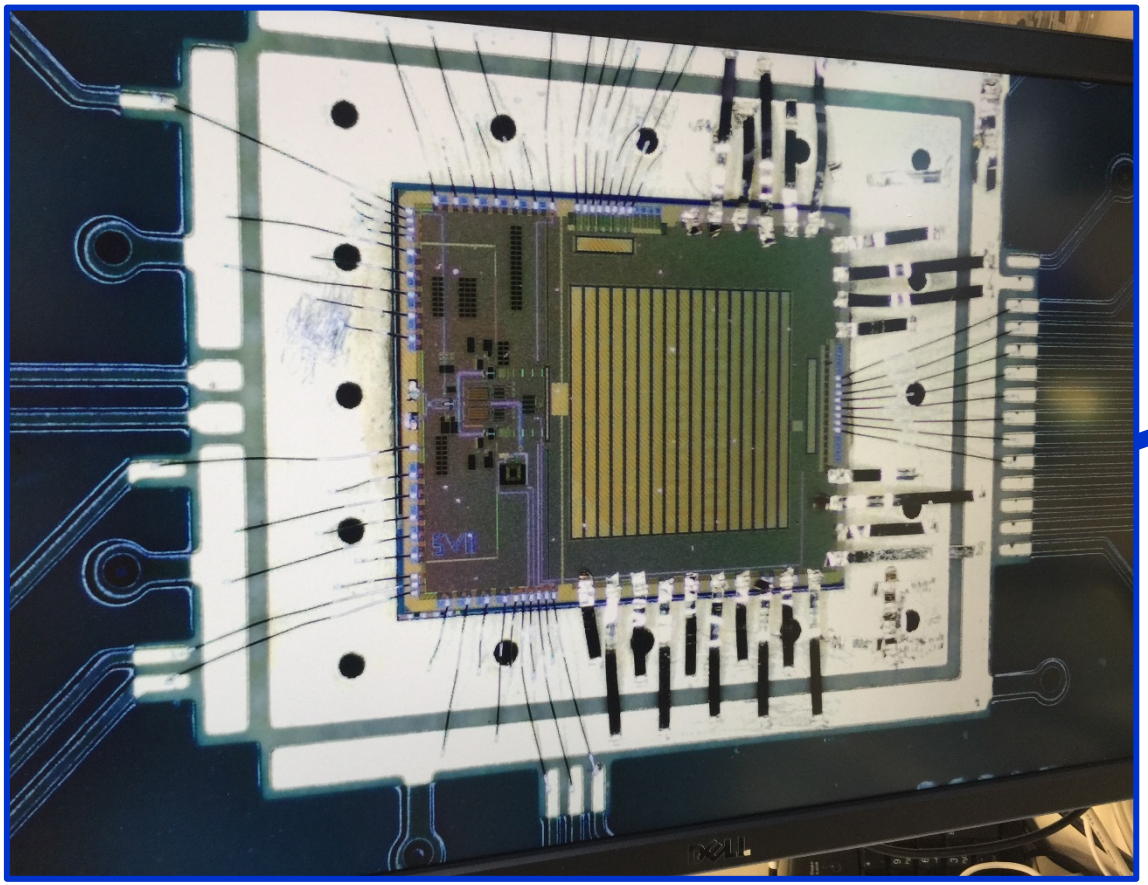


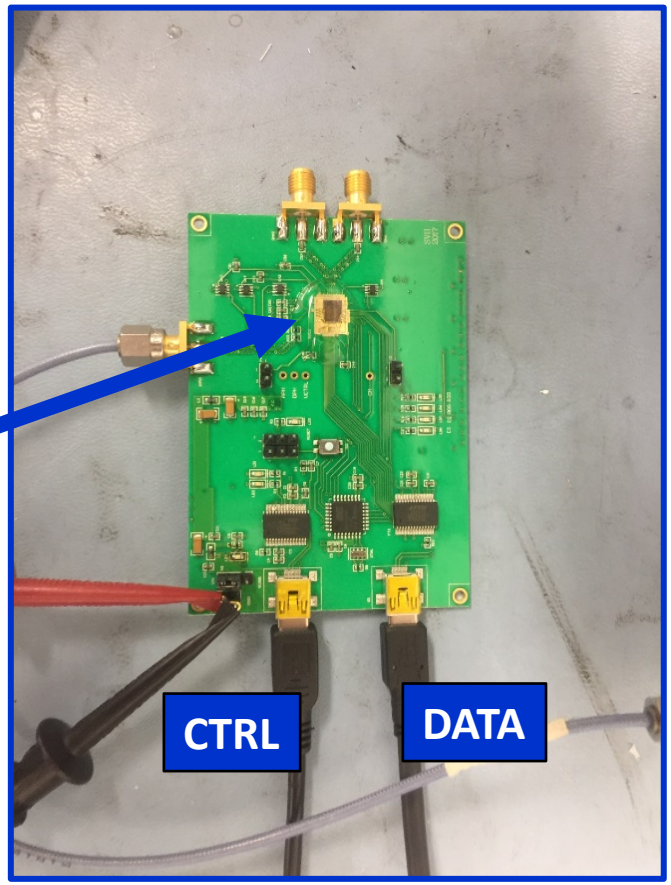
Readout Architecture



- Readout sub-system makes read requests on the PSD core's SRAMS once acquisition is completed and streams them out in one of several programmable formats compatible with USB 1.0 and 2.0 PHYs.
- Optional "3-wire" and I2C formats are selectable to reduce the wiring count of the readout for large arrays.
- Readout clock can be fed in externally or programmable derived from the main clock generation system.
- A multi-modulus programmable divider allows for the main core clock to be divided anywhere from 128 to 8192X to fit a wide range of interfaces and control host options.

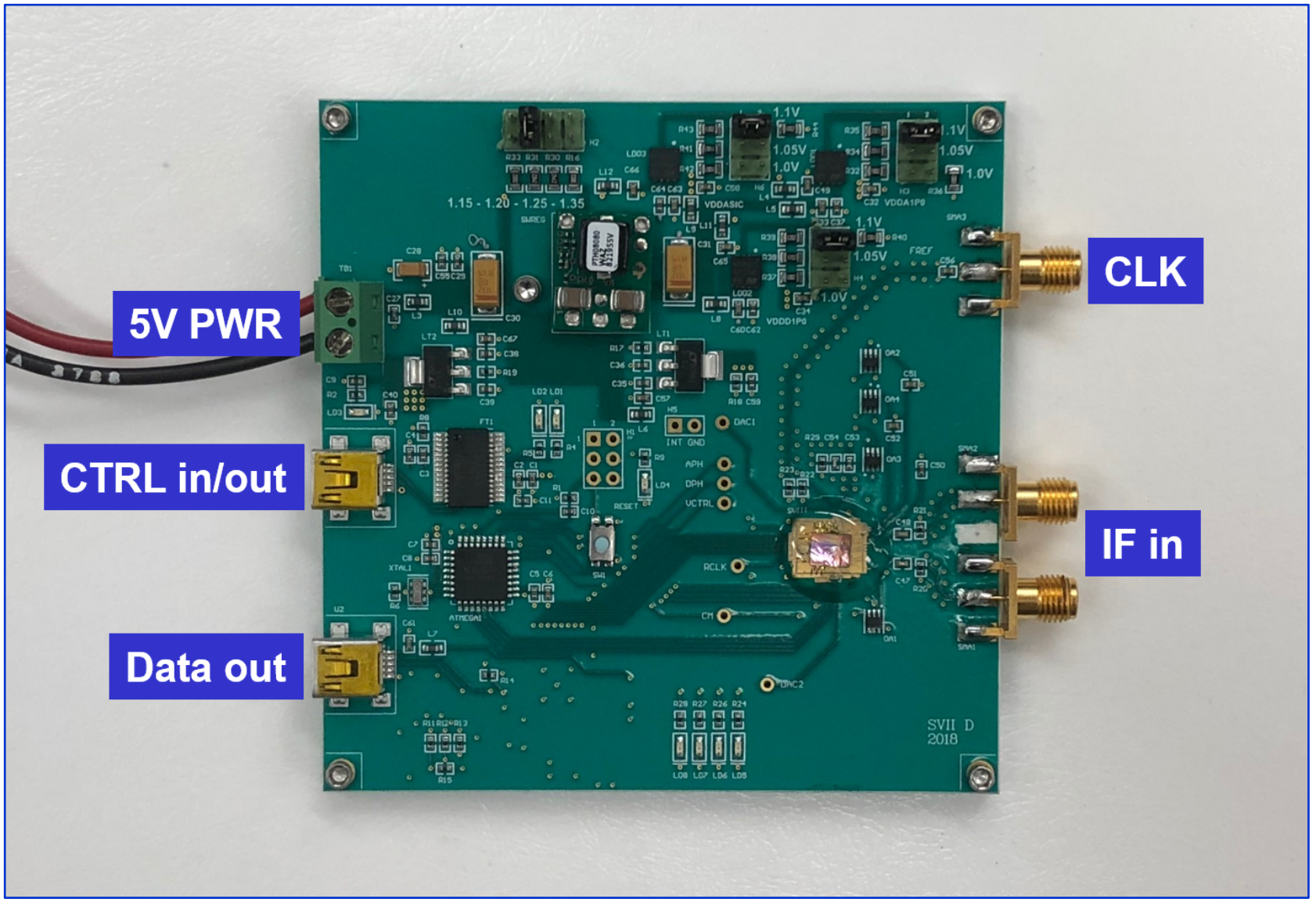
Packaging and Assembly





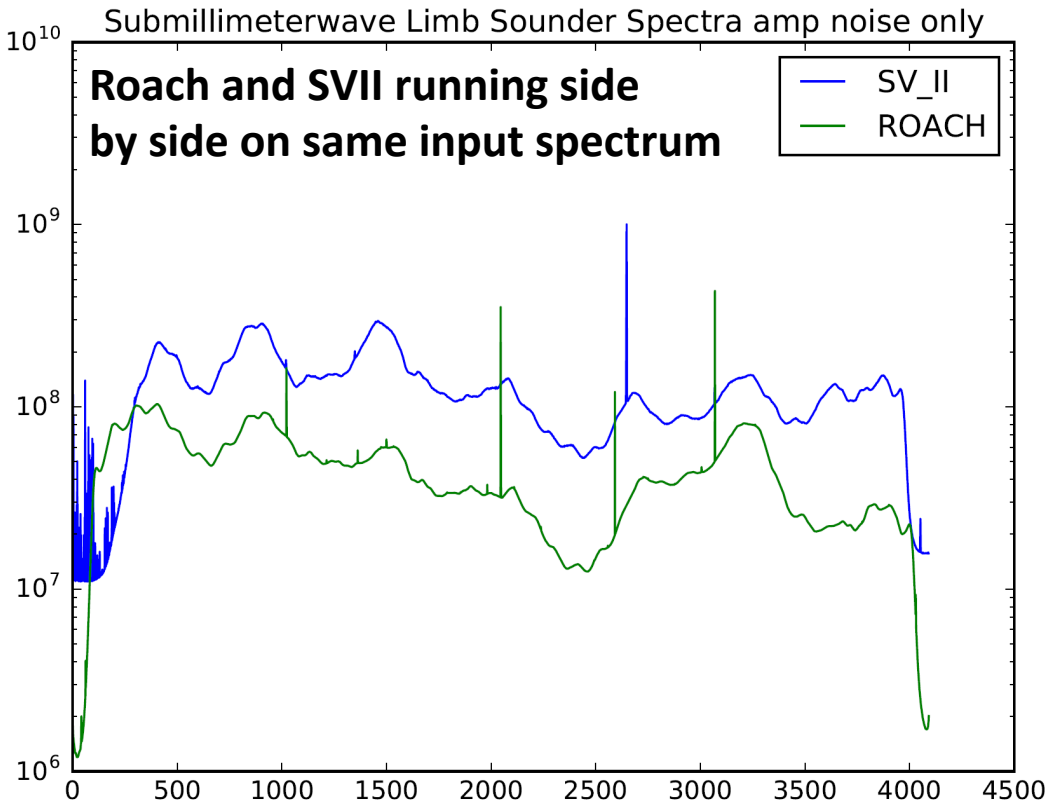
- Developed a simple PCB with USB 2.0 PHY and a micro-controller that interacts with the calibration sub-processor portion of the SoC to manage and adjust calibration firmware, schedule and algorithms.
- Use cheap, reliable ribbon bonds for the high-current supply connections.

Packaging and Assembly



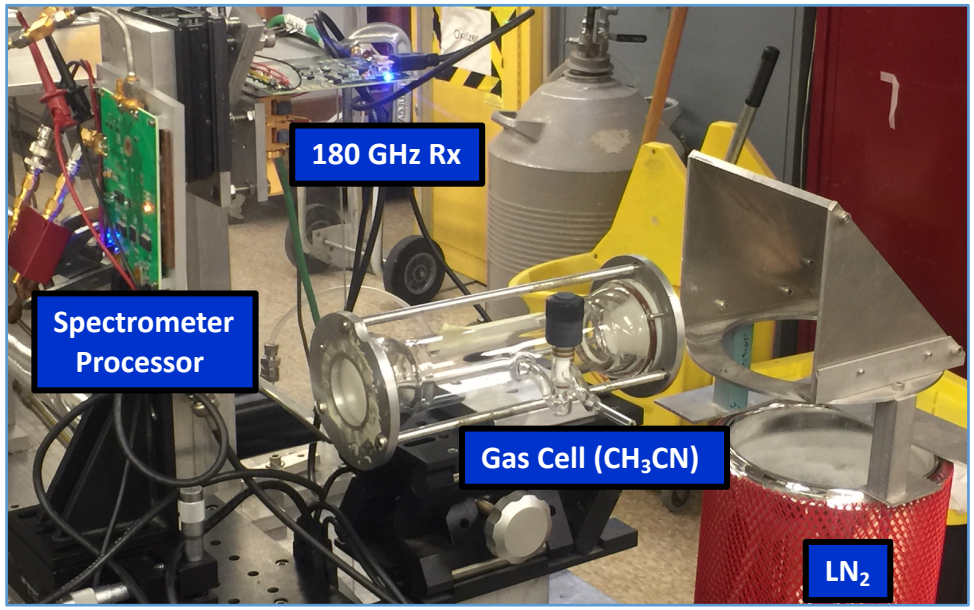
Example Testing – Comparison to JPL ROACH

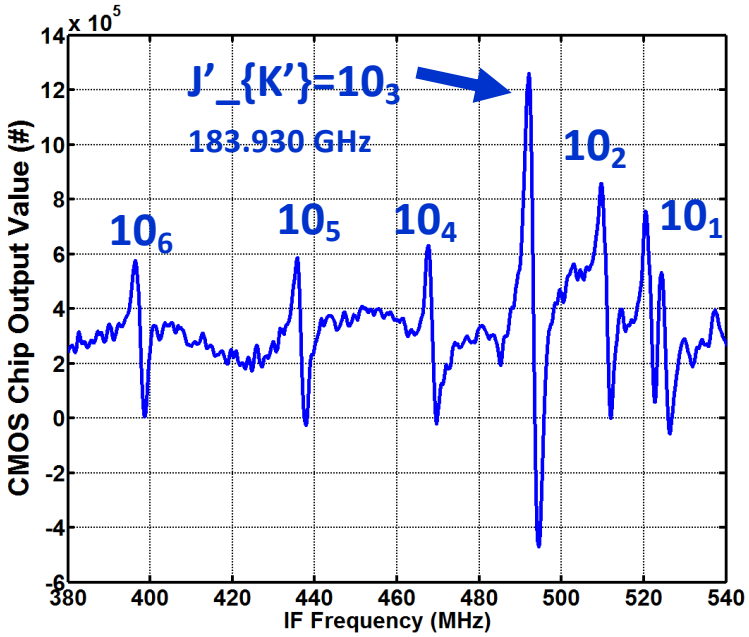
SoC Total Power Breakdown	
PROCESSSOR SUB-SYSTEM	78%
FFT Buttefly Logic	210 mW
FFT Clock Infastructre	255 mW
FFT Reordering Logic	115 mW
Accumulator Logic	33 mW
Accumulator SRAMS	122 mW
Stream Demuxing	88 mW
USB Readout Block	18 mW
Clock division/Prescalers	155 mW
Global Clock Management	225 mW
ADC SUB-SYSTEM	14%
Track and Hold	19 mW
Input Calibration	17 mW
Preamplifier	44 mW
Refrence Generator	26 mW
Interleave Clock Management	120 mW
CLOCK AND CALIBRATION	8%
Internal Synthesizer	62 mW
Clock Pre-scaling	24 mW
Lock Monitoring	15 mW
Total Measured DC Power	**1548**



- **Performs pretty-much identically to the existing JPL ROACH boards, but with much less DC power.**
  - →**Thanks to Robert Stachnik at JPL for helping us to do this direct comparison with his SLS instrument.**

Testing – Gas Cell Measurements (CH_3CN)

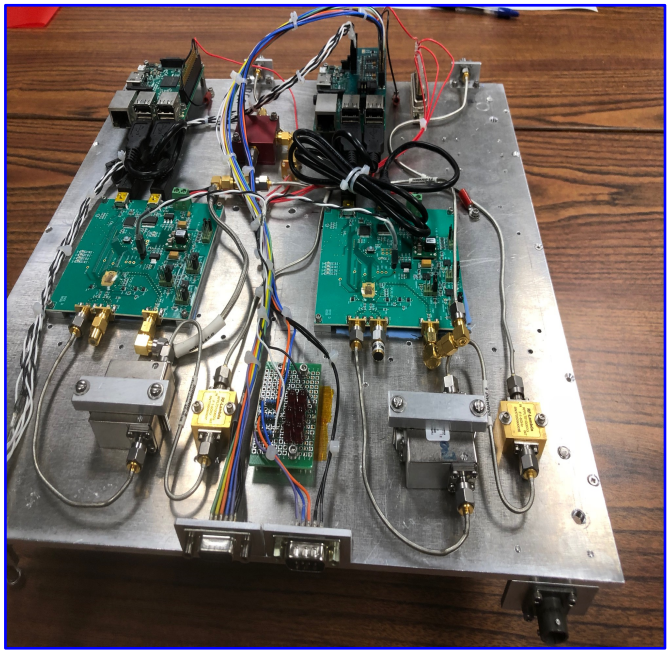


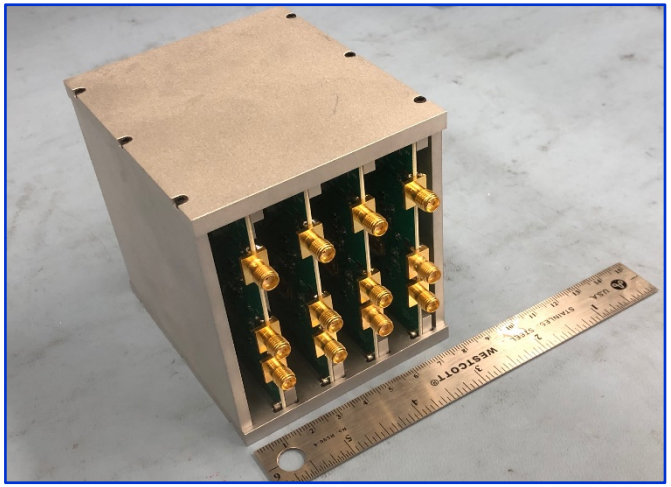


- Paired the CMOS spectrometer processor with a receiver system (a CMOS/InP hybrid receiver) and performed some gas cell measurements at 183 GHz using a switched frequency LO for calibration.

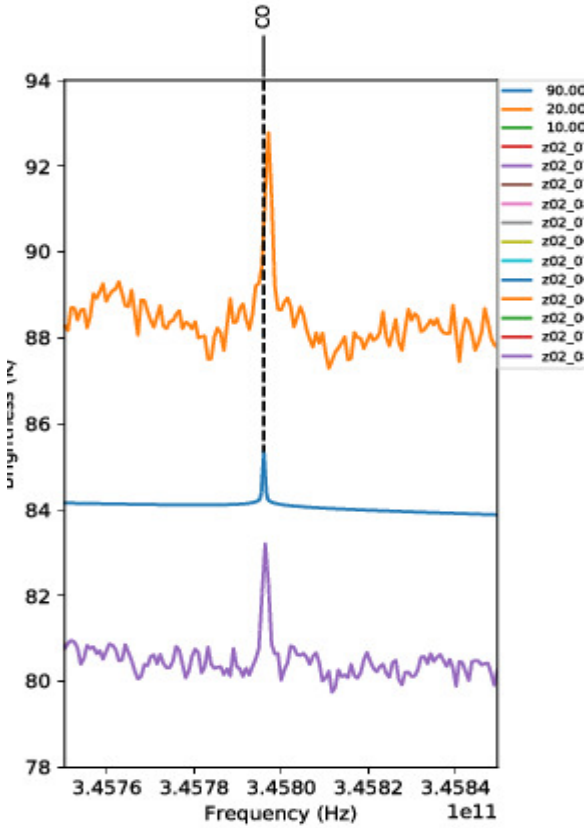
- Above example shows a detection CH3CN (which has multiple lines near 183 GHz)

Instrument Example – Inside CAMLS!

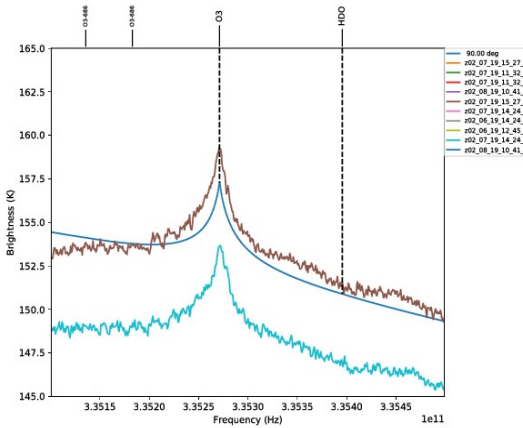




Mesospheric CO line

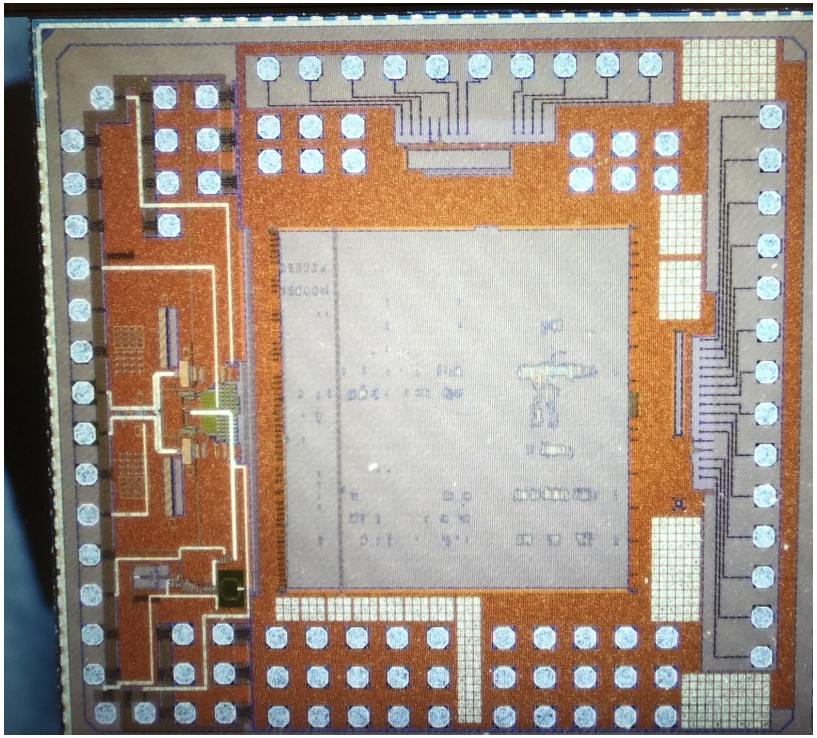


O_3 line



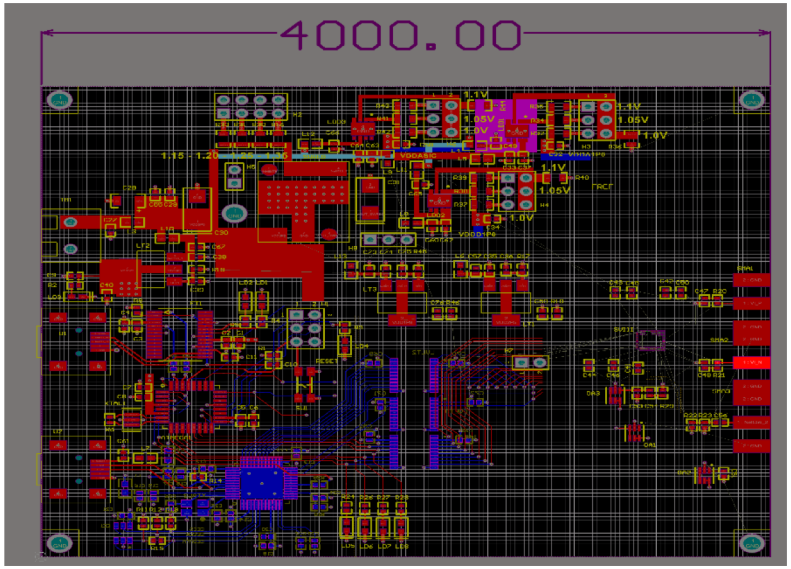
Thanks to Robert Stachnik and the CAMLS team for sharing these measurements.

Assembling Now - SVIII 28nm HPC Version

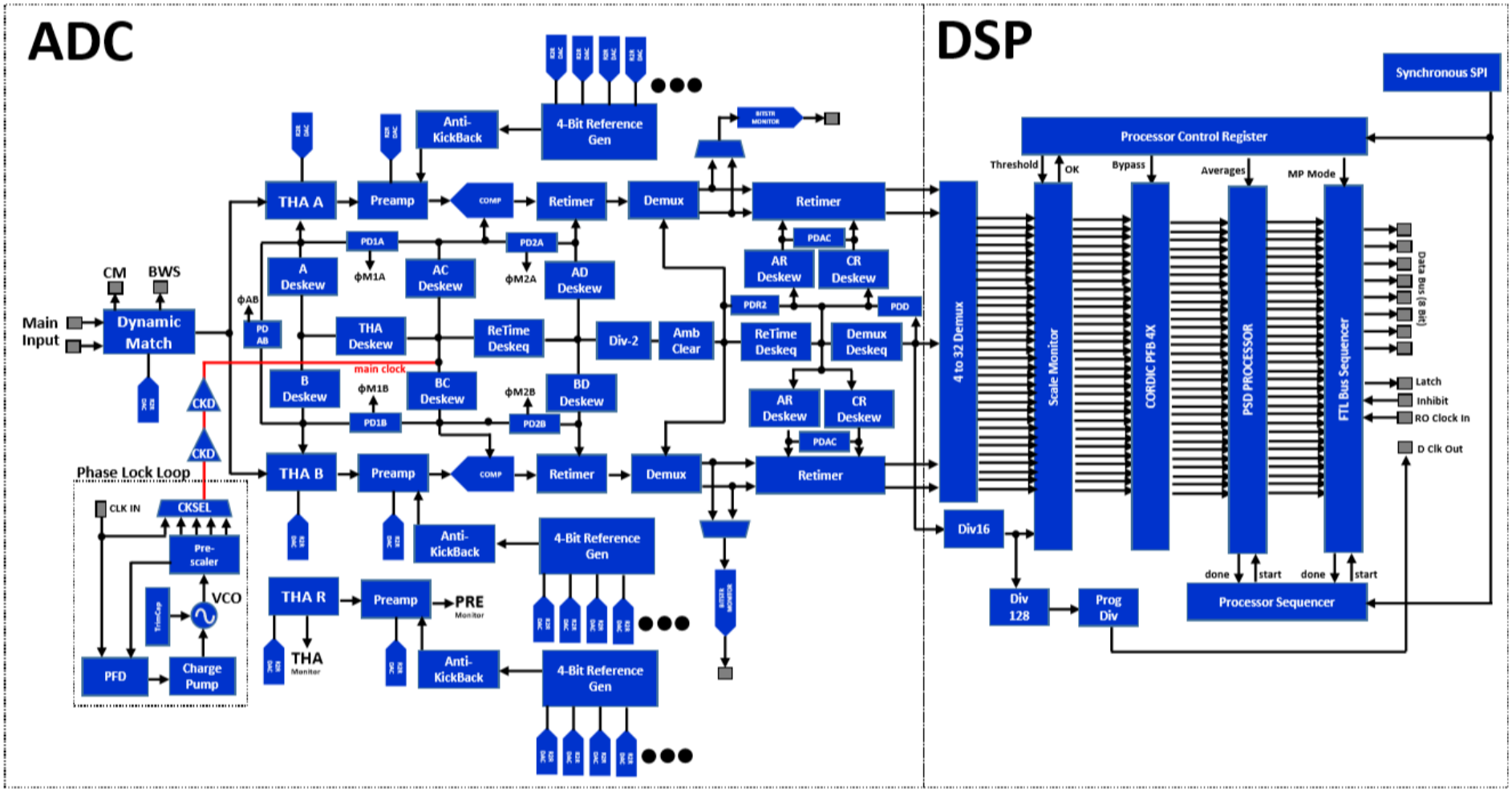


- The chip is fully fabricated and assembly will begin as soon as I get back to JPL after ESTF2019.
- Also we need the students to write *all* the drivers and software and stuff that makes it go.

- PCB design work is done and waiting on a 5-day fabrication cycle… should be back by the time I get home.



Coming soon: SVIII 28nm HPC Version



Summary

- SoC technology dominates over FPGA technology, with drastic reductions of 20-50X in each of size weight and power with no performance impact.

- The key to making these systems perform well and robustly is to use complex calibration systems with dedicated sub-processors and clever software for the calibration and alignment tasks.

- Thanks to support from the NASA Astrophysics Research/Analysis Program as well to the CAMLS IIP that conducted the first field tests of the SVII!